

Fig. 1

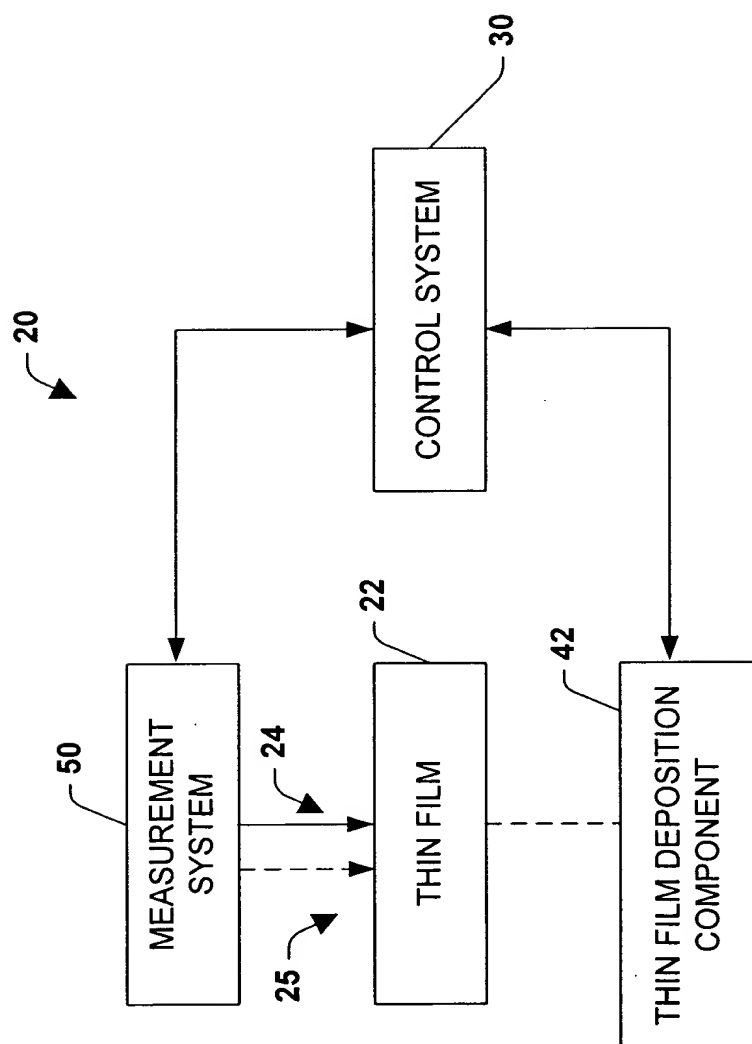


Fig. 2

Fig. 3 is a block diagram of a thin film deposition system 20. The system 20 includes a processor 60, a memory 70, a power supply 78, a light source 62, a sound source 64, a scatterometry system 52, an acoustic system 54, a measuring system, a thin film deposition driver system 80, and a deposition component 40. The processor 60 is connected to the memory 70 and the power supply 78. The processor 60 is also connected to the scatterometry system 52 and the acoustic system 54. The scatterometry system 52 and the acoustic system 54 are connected to the measuring system. The thin film deposition driver system 80 is connected to the processor 60 and the deposition component 40. The deposition component 40 is connected to the substrate 30.

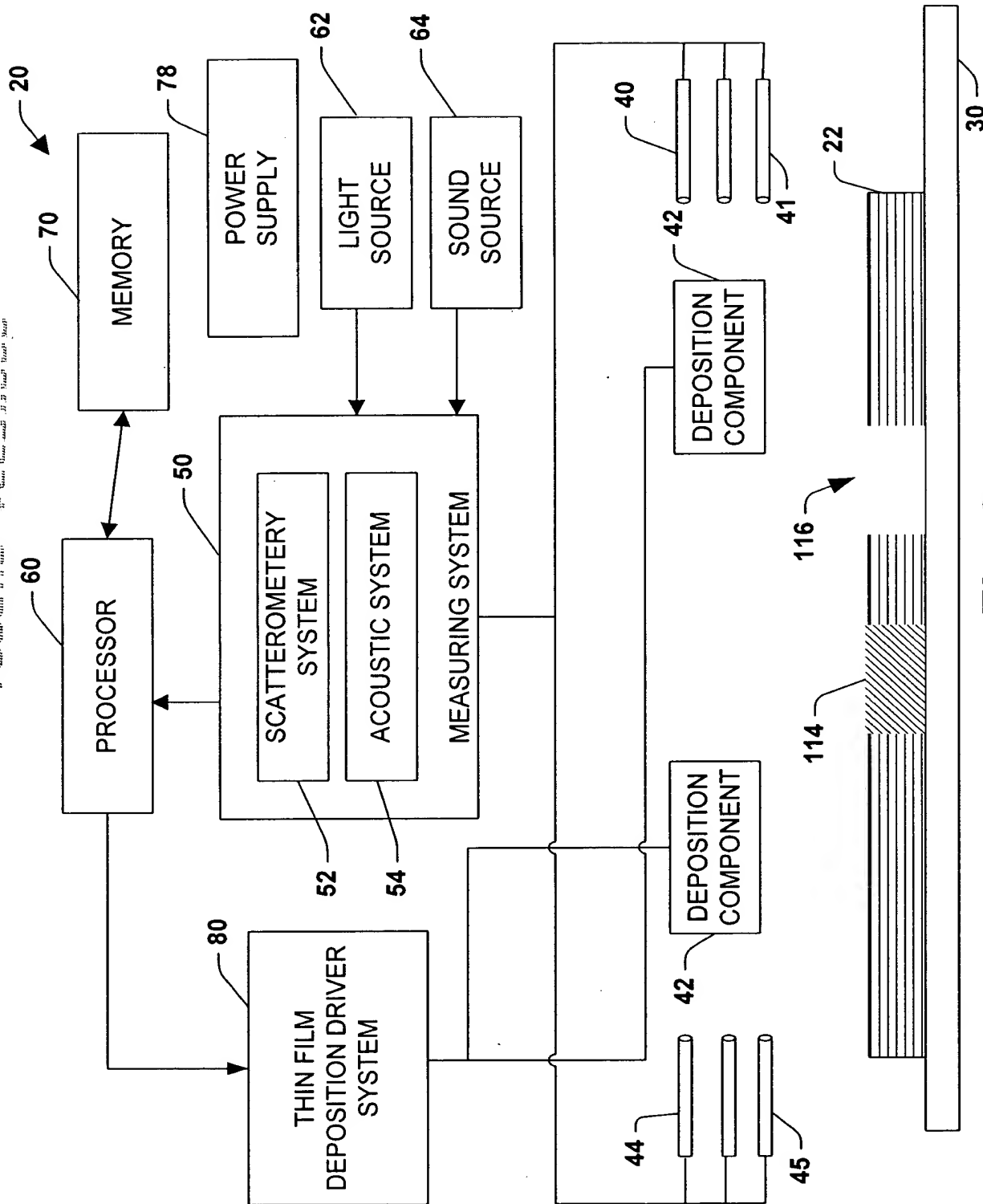


Fig. 3

FIG. 4 is a schematic diagram of a system 20 for measuring a property of a material 22. The system 20 includes a processor 60, a measuring system 50, and a light source 62. The processor 60 is connected to the measuring system 50, which is connected to the light source 62. The measuring system 50 includes a first detector 44 and a second detector 40. The light source 62 emits light 46 towards the material 22. The light 46 is reflected by the material 22 and is detected by the first detector 44. The light 46 is also transmitted through the material 22 and is detected by the second detector 40. The processor 60 is configured to process the signals from the first detector 44 and the second detector 40 to determine the property of the material 22.

20

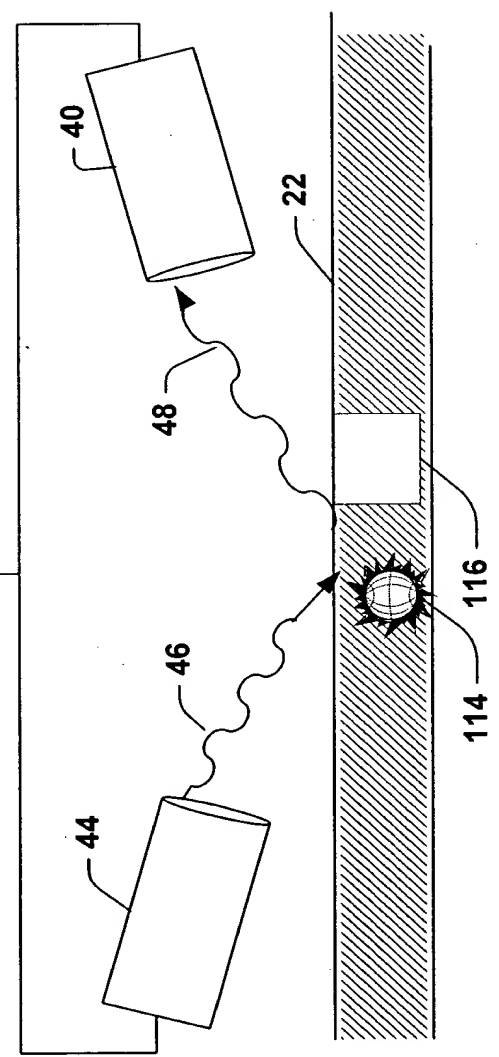
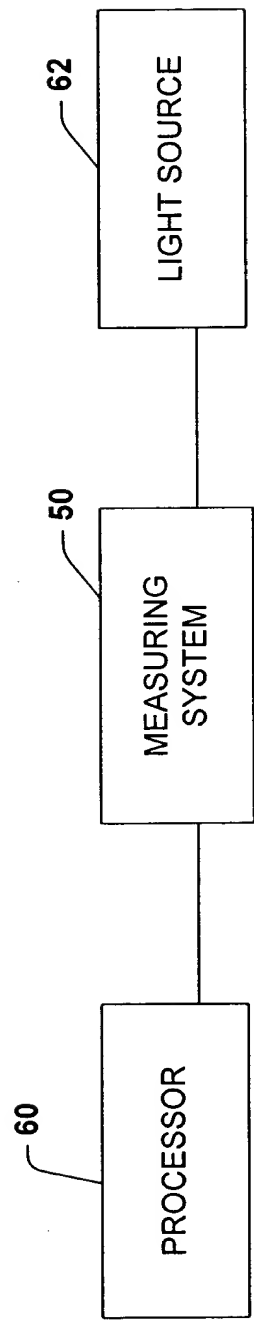


Fig. 4

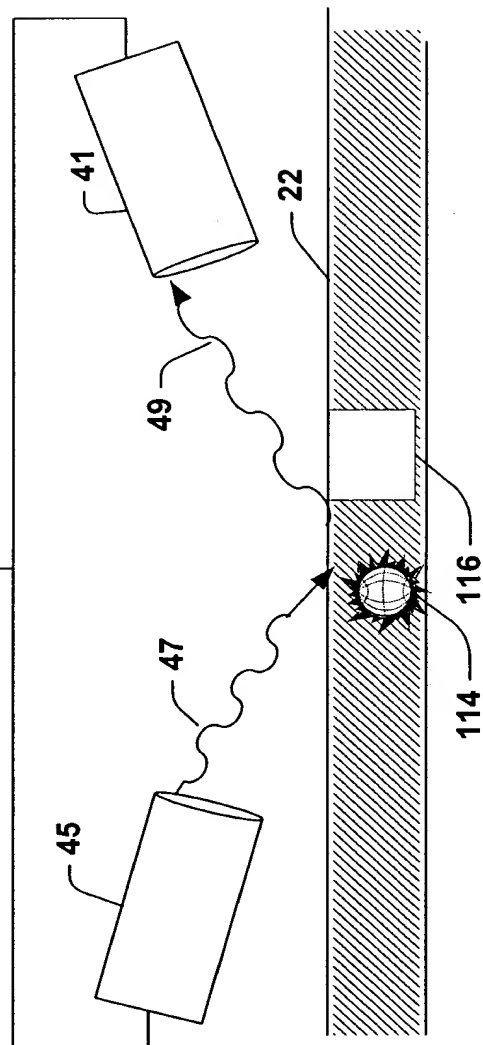
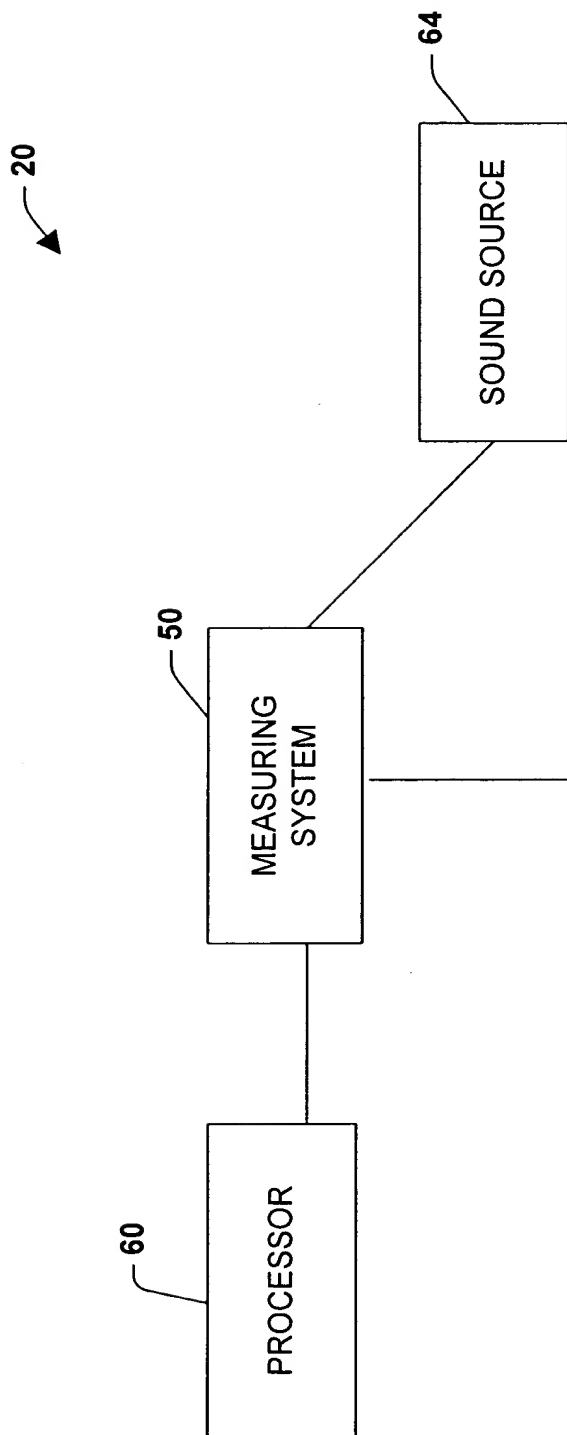


Fig. 5

20

60

PROCESSOR

50

MEASURING
SYSTEM

62

LIGHT SOURCE

64

SOUND SOURCE

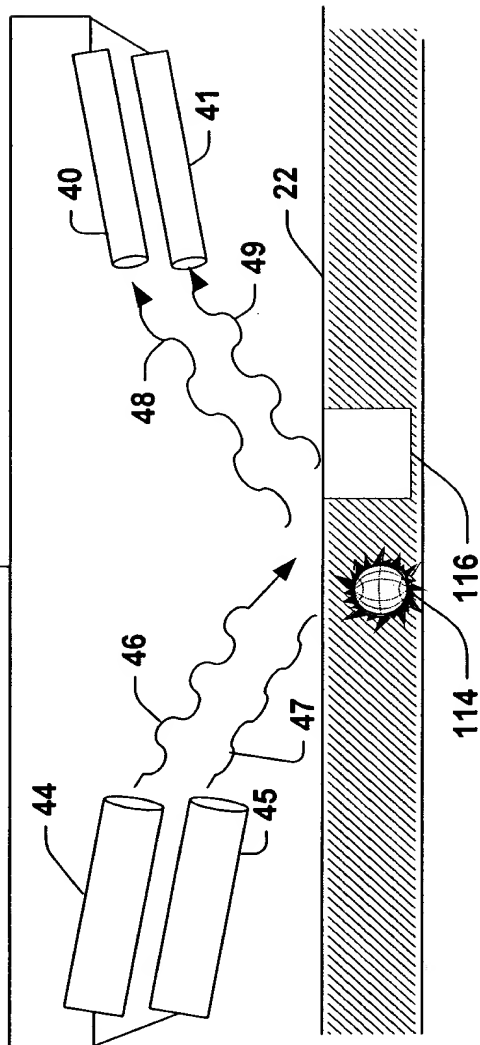


Fig. 6

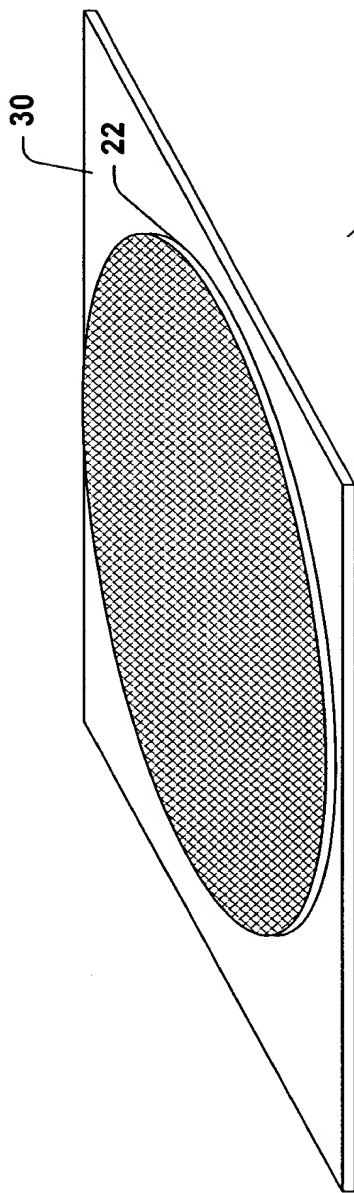


Fig. 7

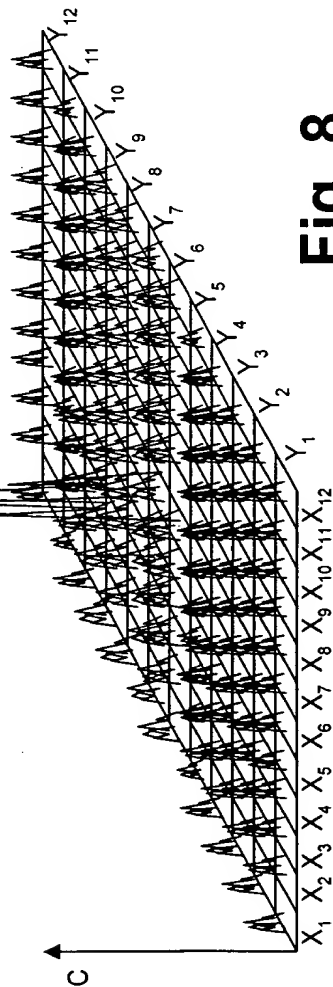


Fig. 8

	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{10}	X_{11}	X_{12}
Y_1	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_2	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_3	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_4	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_5	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_6	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_7	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_8	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_9	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_{10}	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_{11}	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A
Y_{12}	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A	T_A

Fig. 9

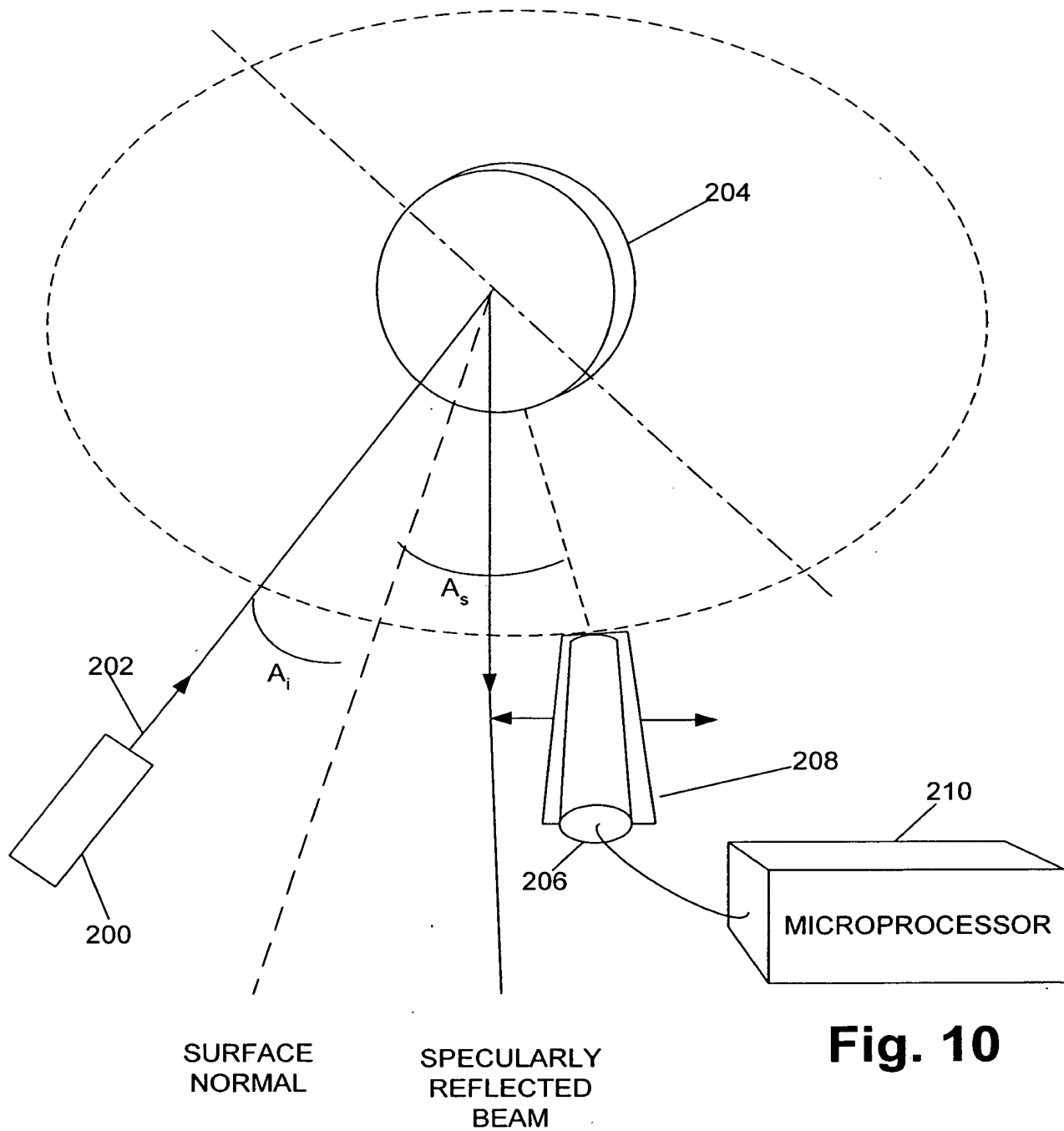


Fig. 10

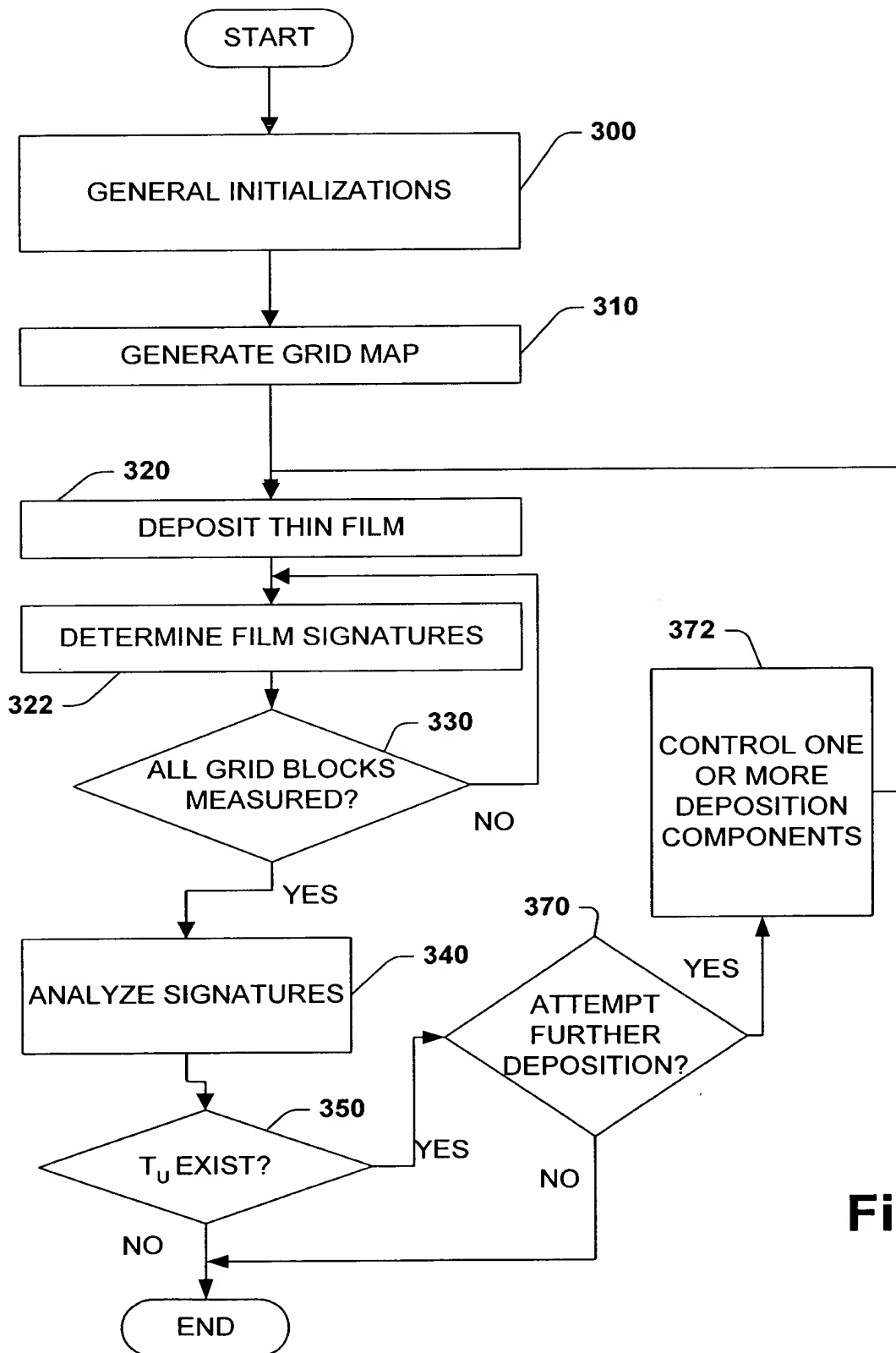


Fig. 11

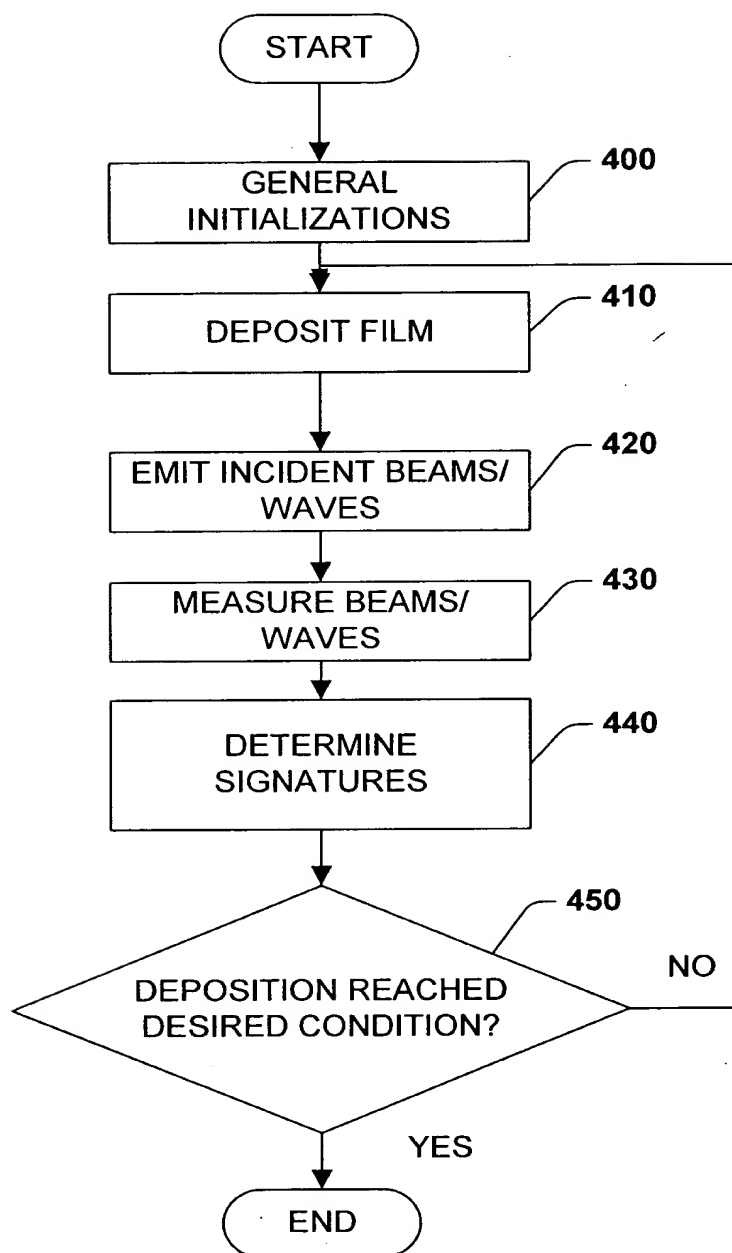


Fig. 12

FIG. 13 is a perspective view of a device 900 in accordance with the present invention. The device 900 includes a plurality of elongated, rectangular elements 902, 904, 906, and 908. The elements 902, 904, 906, and 908 are arranged in a row and are connected to each other by a common structure 910. The device 900 is shown in a perspective view, with the elements 902, 904, 906, and 908 extending away from the viewer. The common structure 910 is located at the bottom of the device 900.

900

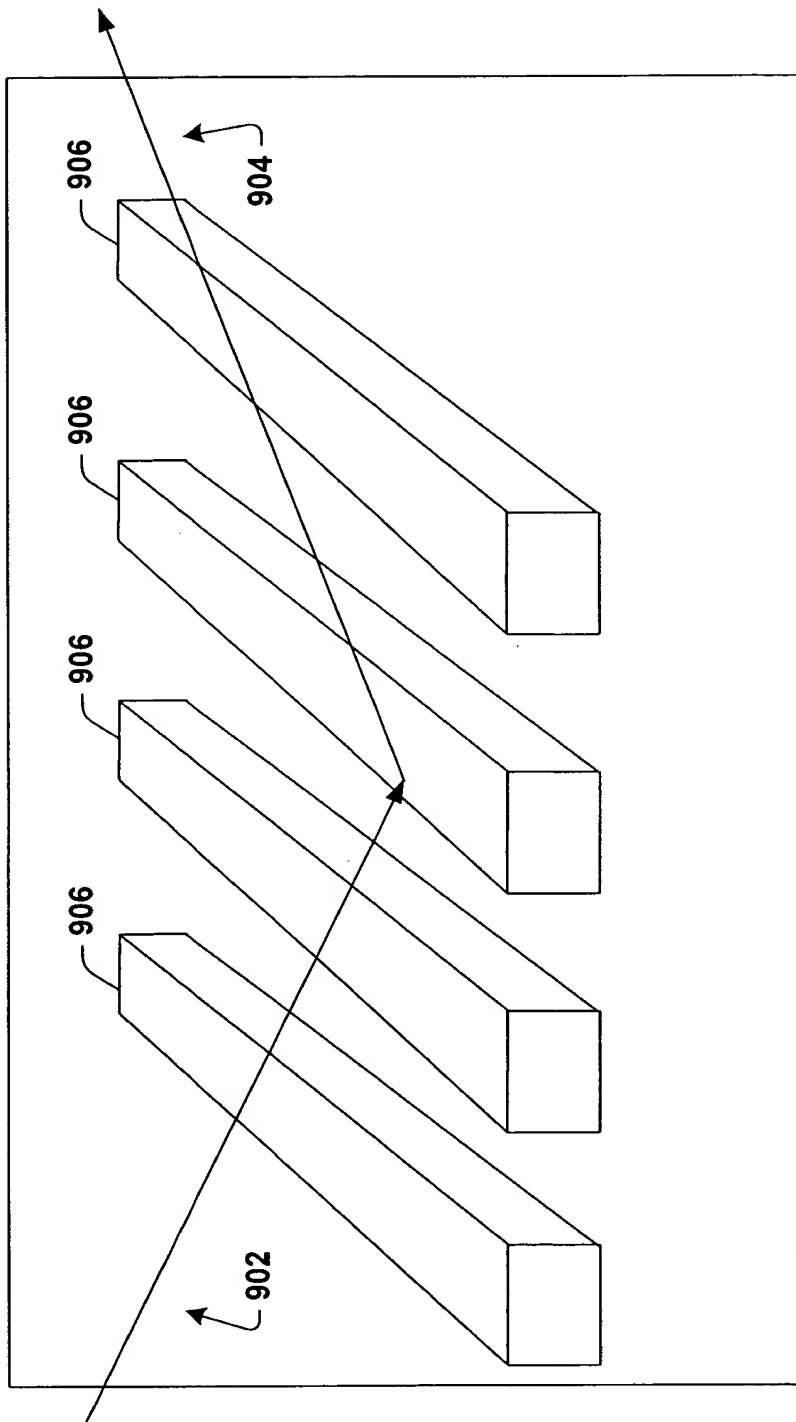


FIG. 13

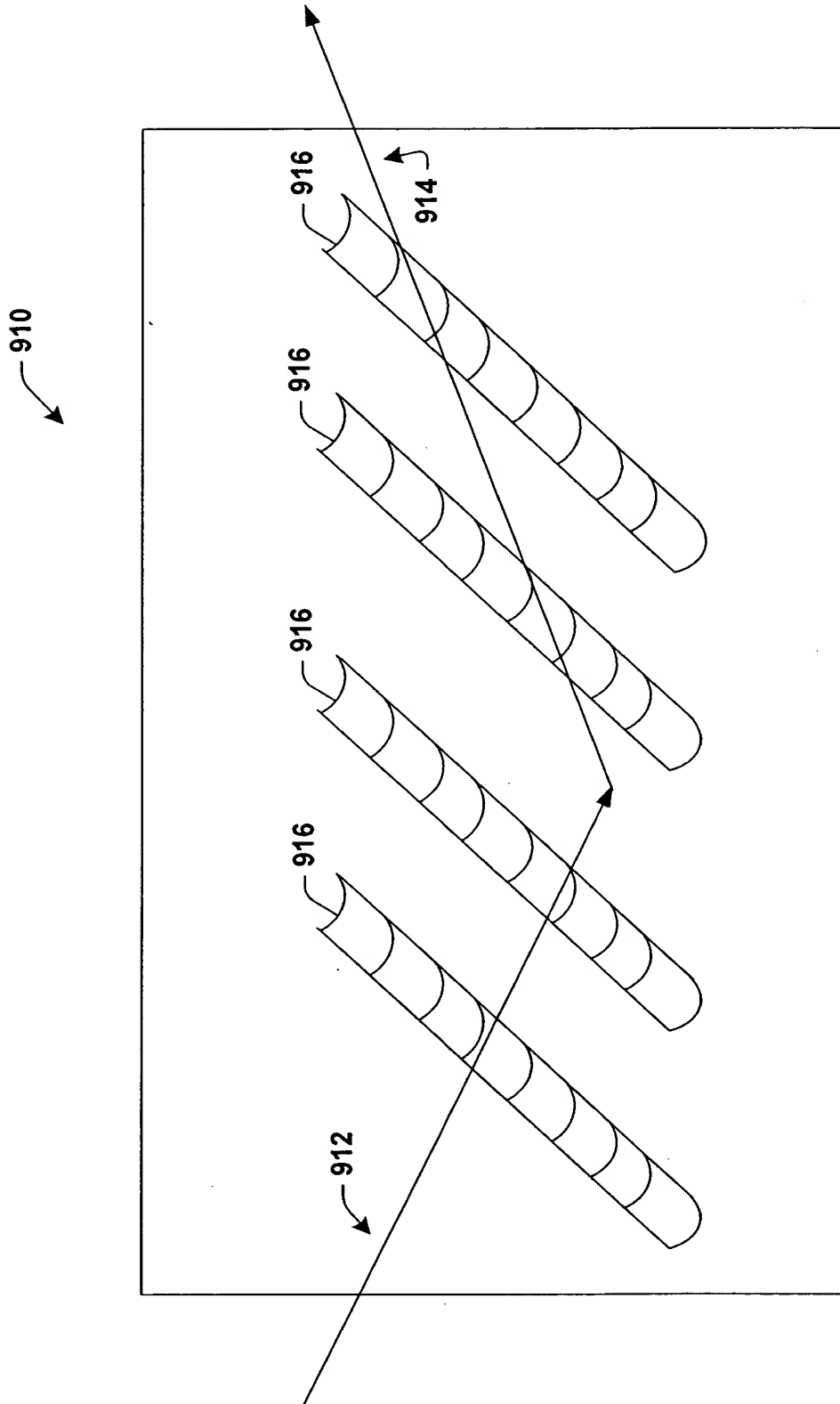


FIG. 14

FIG. 15 is a schematic diagram of a system 900 for processing data. The system 900 includes a data source 902, a data processor 904, a data storage 906, and a data output 908. The data source 902 is connected to the data processor 904, which is connected to the data storage 906. The data storage 906 is connected to the data output 908. The data processor 904 is configured to process data received from the data source 902 and store the processed data in the data storage 906. The data output 908 is configured to output data from the data storage 906.

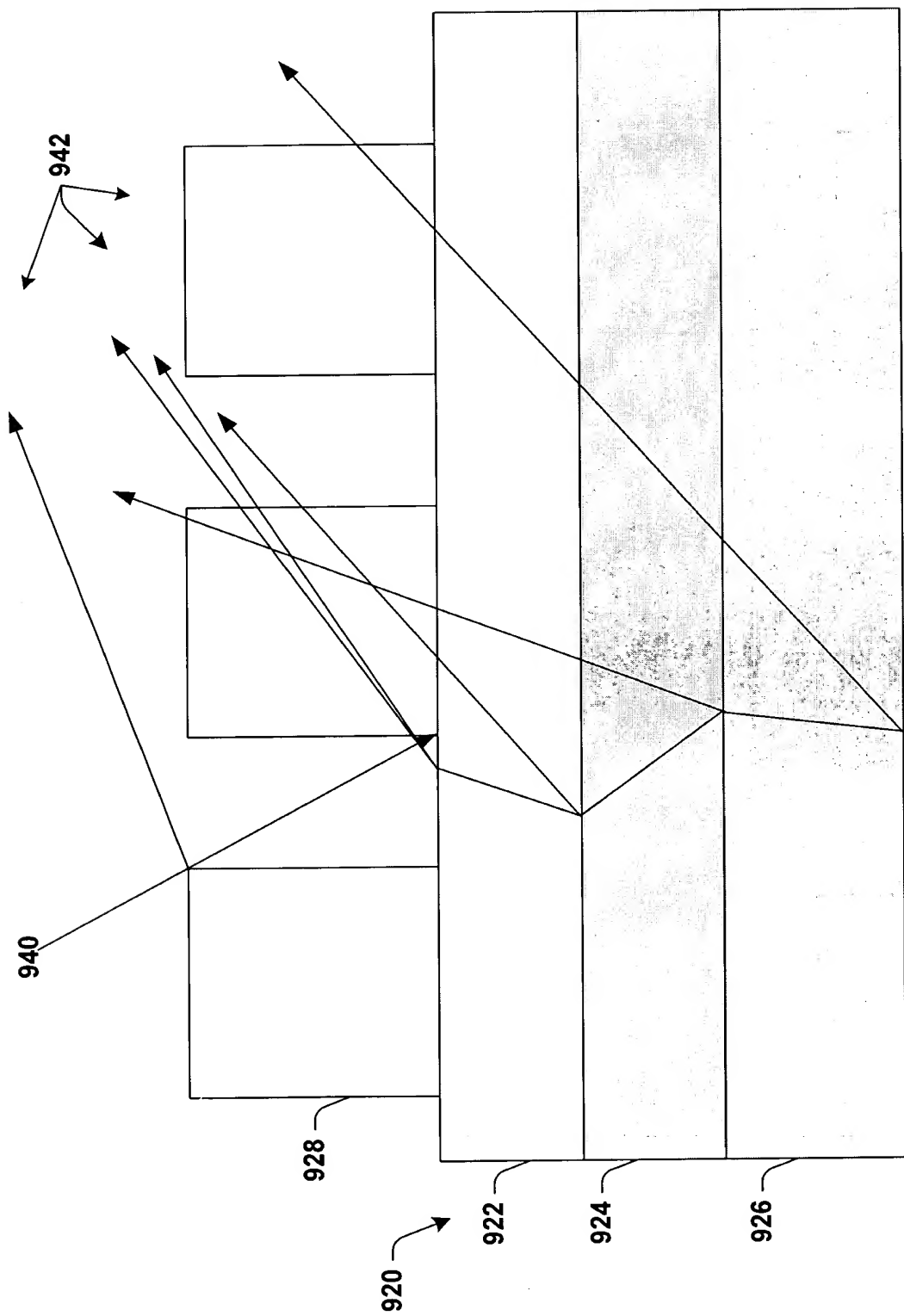


FIG. 15

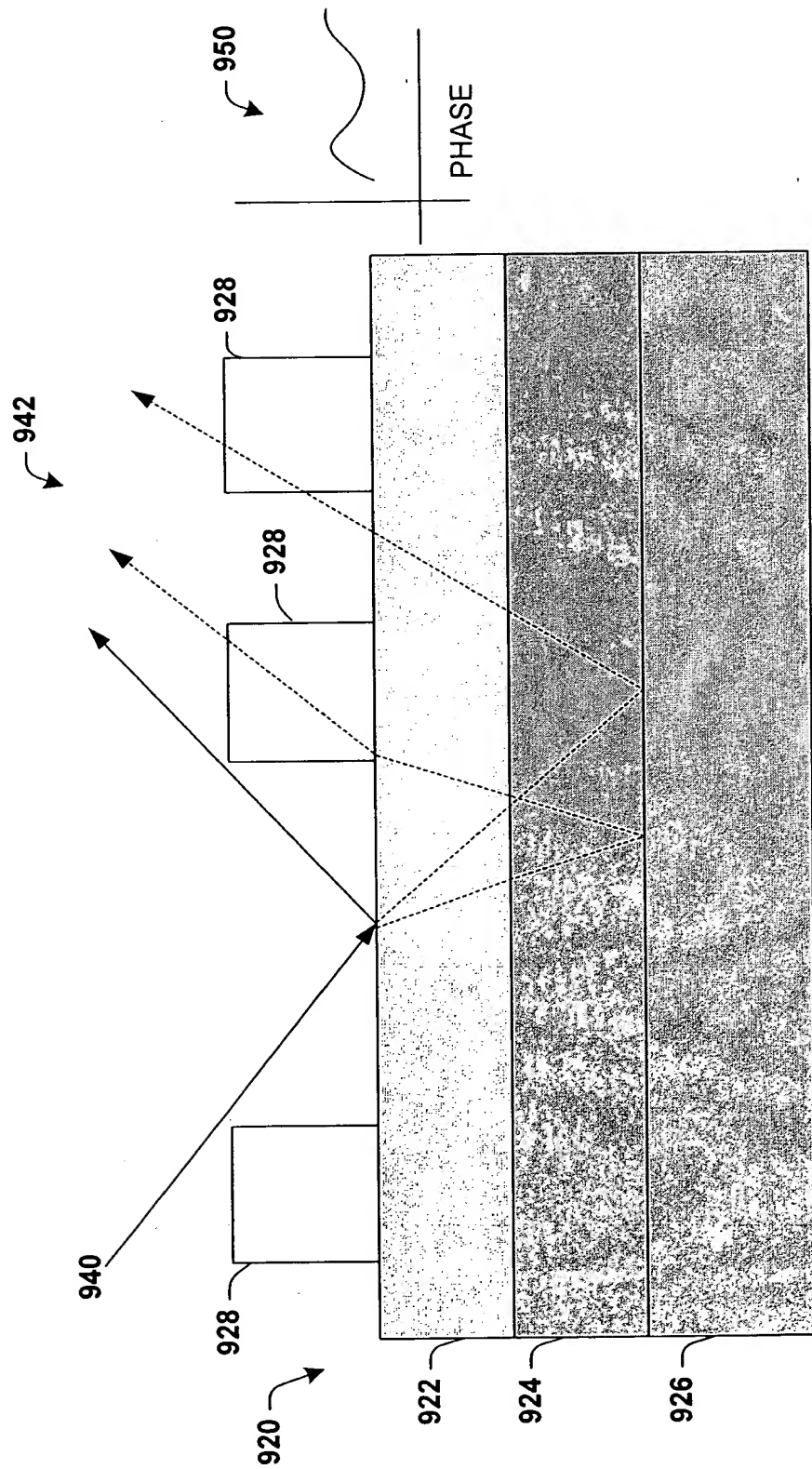


FIG. 16

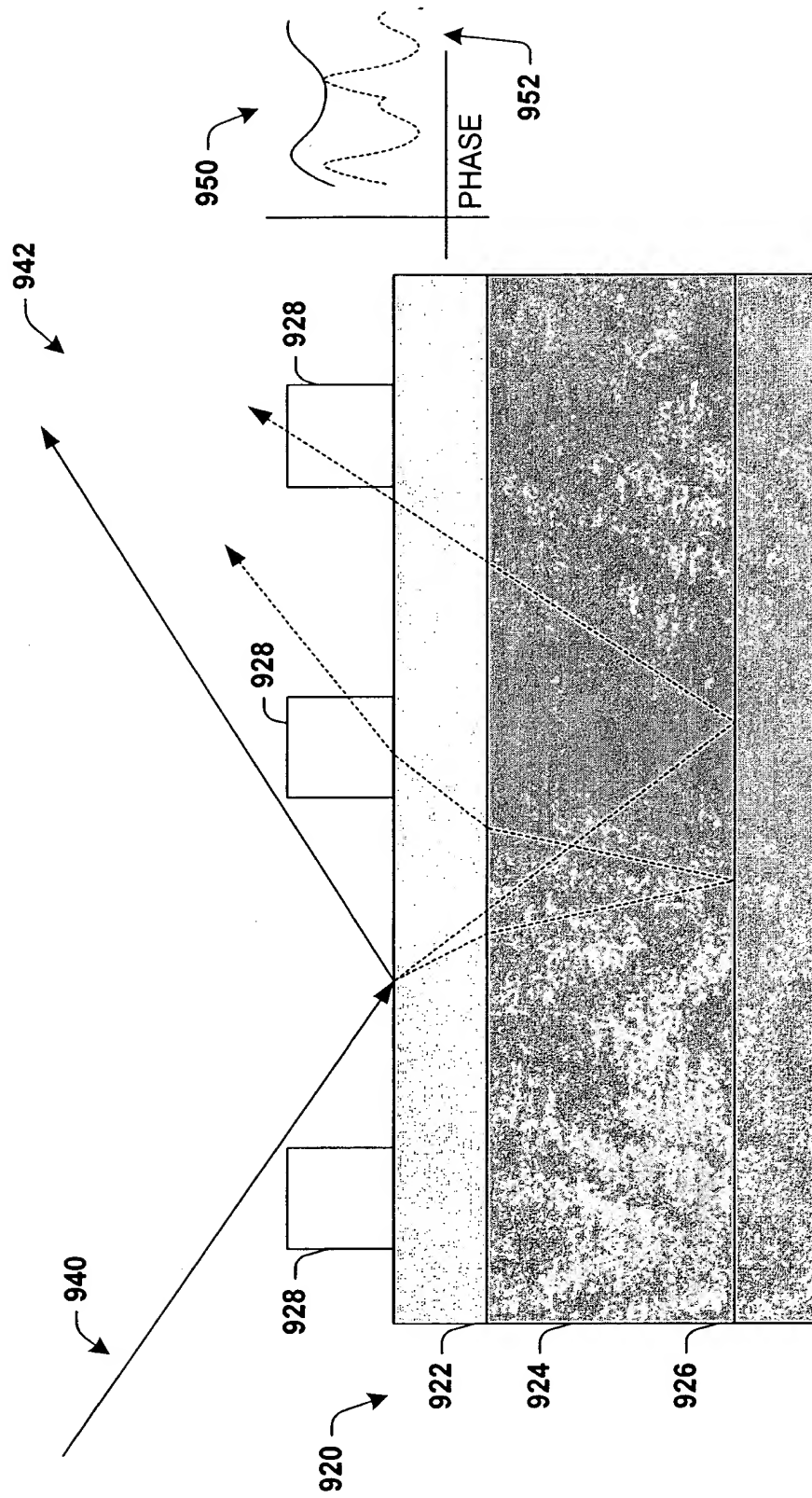


FIG. 17

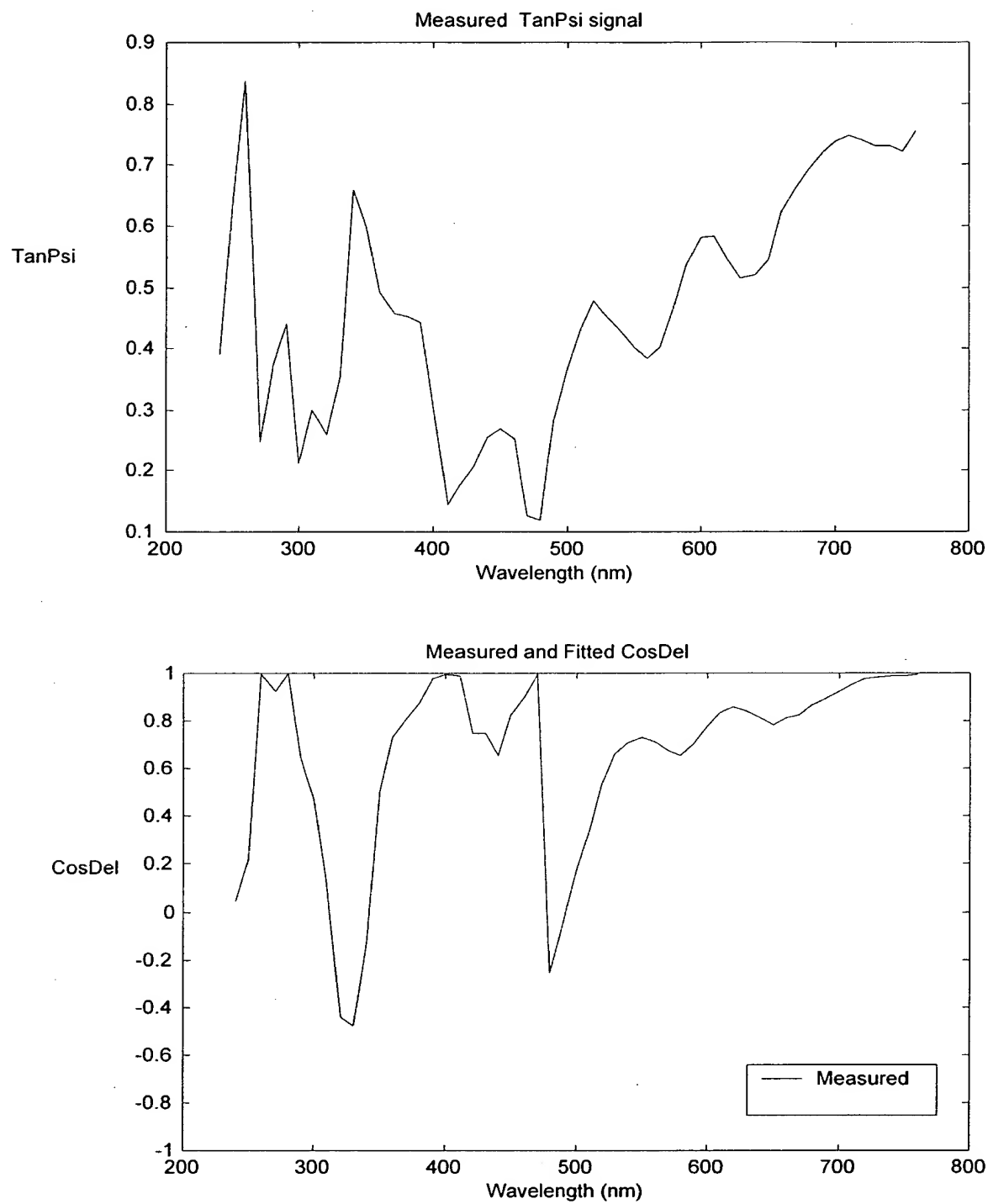


FIG. 18